

# Controlled growth of InAs nanowires on engineered substrates

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We demonstrate the Au-assisted growth of semiconductor nanowires on different engineered substrates. Two relevant cases are investigated: GaAs/AlGaAs heterostructures capped by a 50 nm-thick InAs layer grown by molecular beam epitaxy and a 2  $\mu$ m-thick InAs buffer layer on Si(111) obtained by vapor phase epitaxy. Morphological and structural properties of substrates and nanowires are analyzed by atomic force and transmission electron microscopy. Our results indicate a promising direction for the integration of III-V nanostructures on Si-based electronics as well as for the development of novel micromechanical structures.

## I. INTRODUCTION

Recent years have witnessed the emergence of semiconductor nanowires (NWs) as a new promising platform for nano- and opto-electronics [1, 2]. The small radial extension of the NW structure reduces the strain constraint and allows for novel heterostructure combinations [3, 4, 5, 6]. The strong surface effects during NW growth can lead to high-quality nanostructures from both the crystalline and geometrical point of view [7]. While the vast majority of the present fabrication strategies relies on random deposition processes and marker-aligned metallization of contact electrodes [8], the achievement of a production-oriented NW technology will most likely require a different approach. An interesting possibility consists in the fabrication of vertical devices starting from NWs grown at controlled positions on the surface [9, 10]. The successful development of complex circuits based on vertical NWs, however, will require the development of suitable substrates in order to achieve – for instance – a simple independent and flexible addressing of different NW elements grown on the same chip. More generally, the growth of NWs starting from complex buffer layers or even patterned structures is still in need of a more exhaustive evaluation.

In this paper, we demonstrate the Au-seeded growth of InAs NWs starting from specifically engineered substrates. Two cases are analyzed in Section II and III, respectively: (i) NW growth on a thin InAs layer deposited on top of a GaAs/AlGaAs engineered substrate realized by molecular beam epitaxy (MBE); (ii) NW growth on a 2  $\mu$ m-thick InAs buffer layer deposited on a Si(111) substrate by metal-organic vapor phase epitaxy (MOVPE). While GaAs/AlGaAs substrates are interesting in view of the integration of NWs in high-mobility systems, in the second case we aim at evaluating a possible integration path for III-V nanostructures in Si-based platforms. Both approaches address complex challenges for the substrate engineering such as the growth of buffer layers on

(111) III/V substrates and the formation of antiphase domains on Si.

## II. RESULTS AND DISCUSSION: INAS NWS ON INAS/ALGAAS (111)

GaAs/AlGaAs epitaxy is a well-developed technology that can be used to fabricate complex lattice-matched layered structures and buffer layers are widely used for the growth of high-In containing InGaAs alloys on GaAs substrates. As InAs NWs preferentially grow on the (111)B substrates, the established technology must be adopted to the different substrate orientation. The buffer layer technology is attractive for NWs as heterostructured substrates can also be useful to define thin conducting layers on top of insulating substrates. This is crucial in order to address individual devices in a complicated multi-NW circuit and to reduce stray capacitive couplings. In addition,  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  alloys can have a strong etching selectivity as a function of the composition parameter ( $x$ ) and they can be used to fabricate free-standing micromechanical structures such as membranes and cantilevers [11, 12].

The direct nucleation of InAs NWs on GaAs is challenging [5] and the properties of (111) InAs/GaAs heterojunctions are still largely unexplored. For these reasons we developed a growth procedure to obtain a thin, doped and high-quality InAs layer on top of semi-insulating GaAs/AlGaAs heterostructures. Given the high lattice mismatch ( $\approx 7\%$ ) between (Al,Ga)As alloys and InAs, we opted for the insertion of an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  buffer layer (BL) in the deposition sequence in order to obtain a high-quality InAs top layer [13].

InAs/AlGaAs structures were grown by solid source MBE on GaAs(111)B substrates misoriented by  $3^\circ$  towards the  $[2\bar{1}\bar{1}]$  direction. The layer sequence was chosen in order to be suitable for the fabrication of free-standing micromechanical structures by selective etch-

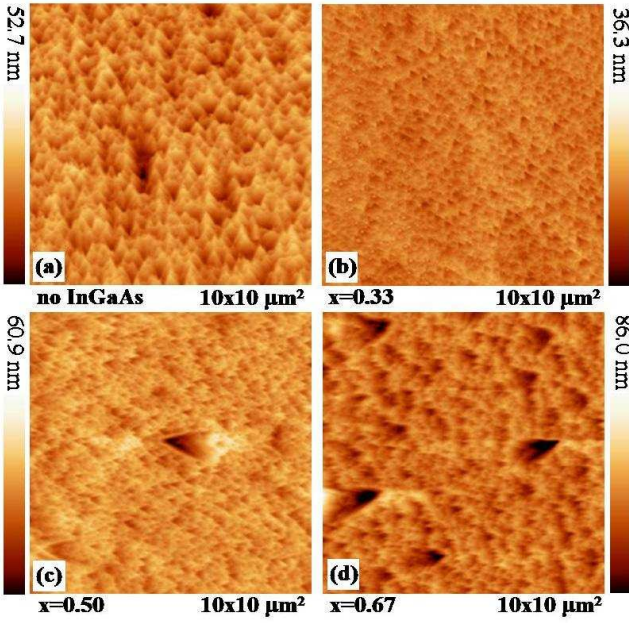


FIG. 1:  $10 \times 10 \mu\text{m}^2$  AFM scans of 50 nm-thick InAs layers grown directly on GaAs(111)B (sample *a*), or after the insertion of a 25 nm  $\text{In}_x\text{Ga}_{1-x}\text{As}$  BL with  $x = 0.33$  (sample *b*, see also Fig. 2a),  $x = 0.5$  (sample *c*) and  $x = 0.67$  (sample *d*).

ing (see supplementary material). Starting from a GaAs(111)B substrate, a 250 nm-thick  $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$  stop-etch layer was grown at 630 °C followed by 1  $\mu\text{m}$  of GaAs grown at 610 °C. The resulting top surface had a typical RMS roughness of  $\approx 0.6$  nm. The InAs cap layer was optimized in terms of strain relaxation, dislocation density and surface roughness. Deposition temperature was selected to be 300 °C, as a trade-off between crystal quality and surface flatness [14]; growth rate and V/III ratio did not have significant effects on the roughness and were selected to be 0.1 nm/sec and 30 (beam equivalent pressure ratio), respectively. The final InAs thickness was 50 nm, since a residual presence of Ga atoms migrating from the substrate was detected at the surface in thinner layers [15], while in thicker layers we observed an increase of the surface roughness. Figure 1 shows a series of atomic force microscopy (AFM) topographic pictures of the top InAs surface for samples with different  $\text{In}_x\text{Ga}_{1-x}\text{As}$  BLs. InAs in sample *a* was grown directly on GaAs and exhibits a surface roughness of  $\approx 6.1$  nm RMS. Such a roughness can be significantly reduced (RMS 3.7 nm) by the insertion of a 25 nm BL with  $x = 0.33$  (sample *b*). We observed that increasing the In content of the BL causes the formation of  $\approx 50$  nm-deep arrowhead-shaped holes, as it can be seen in samples *c* ( $x = 0.5$ ) and *d* ( $x = 0.67$ ), respectively.

Given the lower roughness, sample *b* (see layer sequence in Fig. 2a) was chosen for the investigation of NW growth and studied by bright field transmission

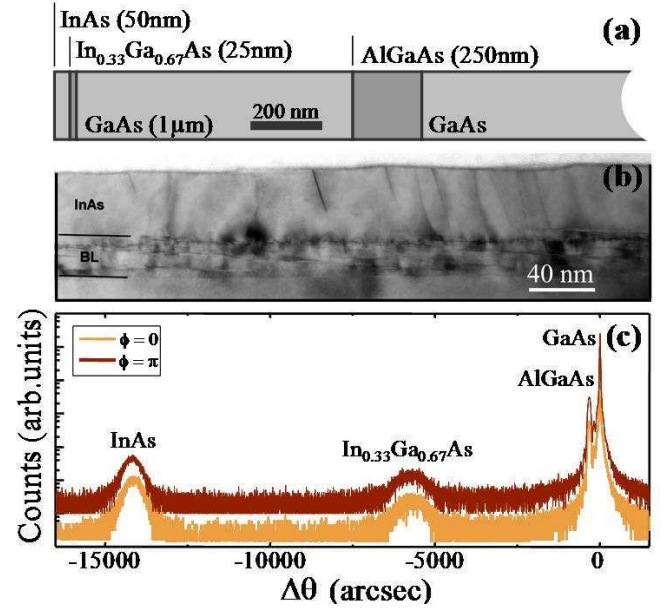


FIG. 2: (a) The layer sequence in the InAs/(Al,Ga)As substrate (sample *b*). (b) Bright field [110] cross-sectional TEM image of sample *b*: defects are located mainly in the BL. In the InAs layer, some threading dislocations are evident as dark segments preferentially along the (211) direction which results from (111) planes in the (110) projection. (c) XRD Bragg scan of sample *b* along two azimuths rotated by 180°.

electron microscopy (TEM). Figure 2b reports an image taken near [110] zone axis in (111) diffraction conditions and demonstrates that defects due to strain are mainly located at the BL. Strain relaxation was assessed by high-resolution X-ray diffraction (XRD) on symmetric (333) reflection at two different azimuths rotated by 180°. Despite the 3° miscut of the GaAs(111)B substrate, Bragg peak positions are virtually identical at the two azimuthal angles, indicating a complete strain relaxation both in the  $\text{In}_{0.33}\text{Ga}_{0.67}\text{As}$  buffer layer and in the InAs top layer. Following van-der-Pauw measurements, the intentionally-doped InAs cap layer was found to have a carrier density and mobility of  $n = 1.7 \times 10^{18} \text{ cm}^{-3}$  and  $\mu = 4.5 \times 10^3 \text{ cm}^2/\text{Vs}$ , respectively.

InAs NWs were fabricated by means of chemical beam epitaxy (CBE) seeded by Au aerosol nanoparticles [16]. Substrates were first annealed and deoxidized at 520 °C for 17 minutes under As pressure; NW were then grown at 425 °C for 60 minutes using trimethylindium (TMIn) and pre-cracked tertiarybutylarsine (TBAs) with respective partial pressures of 0.15 and 1.5 mbar (supply line) as precursors [16]. Figure 3 demonstrates the successful nanoparticle-seeded deposition of NWs on sample *b* (SEM image at 15° tilt). NWs grow normal to the sample surface similarly to what observed on bulk InAs(111)B substrates. NWs had a diameter of  $\approx 60$  nm and the right inset reports a higher magnification view of a single

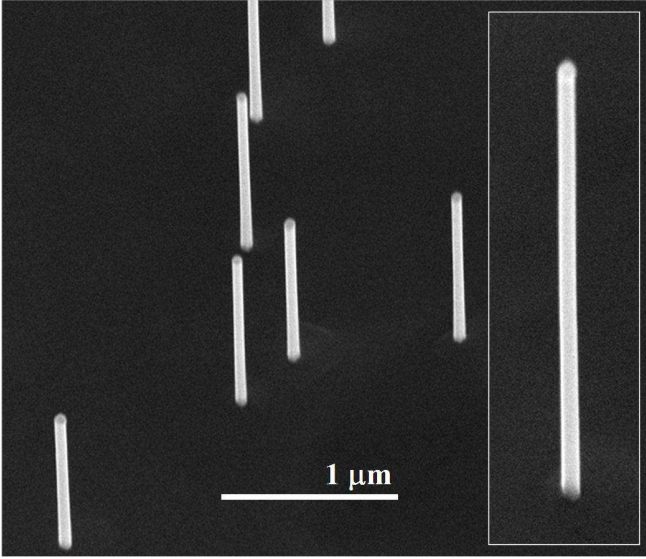


FIG. 3: Main panel: SEM image (tilt  $15^\circ$ ) of InAs NWs grown on an InAs/(Al,Ga)As engineered substrates starting from Au nanoparticles deposited by aerosol technology. Inset: magnification of a single NW.

wire. A statistical analysis of the NW length gives an average value of about  $2.8 \pm 0.4 \mu\text{m}$ , which is  $\approx 25\%$  shorter compared to the one of NWs grown in parallel on a standard InAs substrate ( $3.7 \pm 0.2 \mu\text{m}$ ). Such a difference might be linked either to a different surface mobility for In on the InAs(111)B cap layer of sample B in comparison with a bulk InAs(111)B substrate or to difficulties in the nucleation process. Despite this, our study shows these substrates are well-suited for NW growth.

### III. RESULTS AND DISCUSSION: INAS NWS ON INAS/SI(111)

The growth of III-V semiconductors on Si has attracted significant research efforts in the past decades as it holds the promise of a straight-forward integration of high-mobility and optically-active materials on top of the mainstream low-cost Si-based electronics. Due to the extreme difficulties linked to the high lattice mismatch between these materials however very few studies have been reported on the deposition of InAs on top of a Si substrate because of severe issues such as the formation of dense dislocations networks, thermal cracks and anti-phase domains (APD) [17]. While cracks can be easily identified by optical microscopy, APDs are not so easy to detect and can form as a consequence of growth of polar III-V material on top of the non-polar Si surface. In the case of a Si(111) substrate, resulting III-V layers can contain at the same time some portions of surface oriented in the (111)A and others in the (111)B direction.

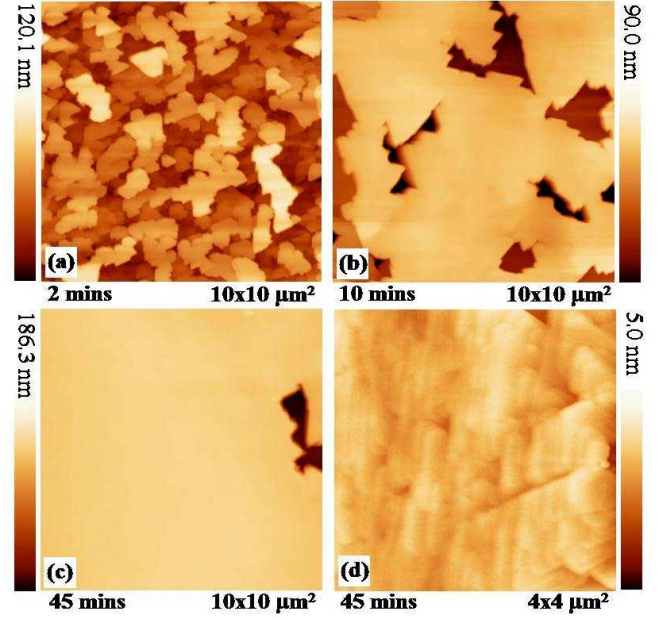


FIG. 4: AFM images of the surface after the second growth step as a function of growth time: (a) 1 minute, (b) 10 minutes, (c) 45 minutes and (d) zoom-in of panel (c). RMS in the last scan is 2.2 nm.

As demonstrated in the following paragraphs, our epitaxial procedure preferentially develops (111)B-oriented domains and InAs NWs grow in the vertical direction.

InAs buffer layers were deposited directly on Si(111) substrates by MOVPE using a two-step procedure described in detail in Ref. [18]. After the growth of a first nucleation layer of Stranski-Krastanow islands, a second growth step was used to reconstruct a flat layer of good morphological and conducting properties. Figures 4a-d display the surface structure as a function of the growth time during the second step. AFM images indicate that the InAs layer grows via a mechanism of triangular nuclei extension, probably limited by the diffusion length of the group III ad-atoms on the surface [18]. For InAs layers thicker than  $\approx 1 \mu\text{m}$ , the surface is characterized by large regions of small roughness (2.2 nm), even if portions with larger roughness could not be completely eliminated (see right side of Fig. 4c). The InAs layer on which NWs were grown was obtained by a 180 minutes deposition and had a total thickness of approximately  $2 \mu\text{m}$ . This unintentionally doped substrate was also characterized by vander-Pauw measurements. Carrier density and mobility at room temperature was measured to be  $n = 9 \times 10^{16} \text{ cm}^{-3}$  and  $\mu \approx 5 \times 10^3 \text{ cm}^2/\text{Vs}$ , respectively.

Figure 5a shows a  $30^\circ$ -tilted SEM image of InAs NWs grown on the  $2 \mu\text{m}$ -thick InAs/Si substrate following the same procedure indicated in the previous section, but with a shorter deposition time (30 minutes). The growth process is normal and the NWs had a length of



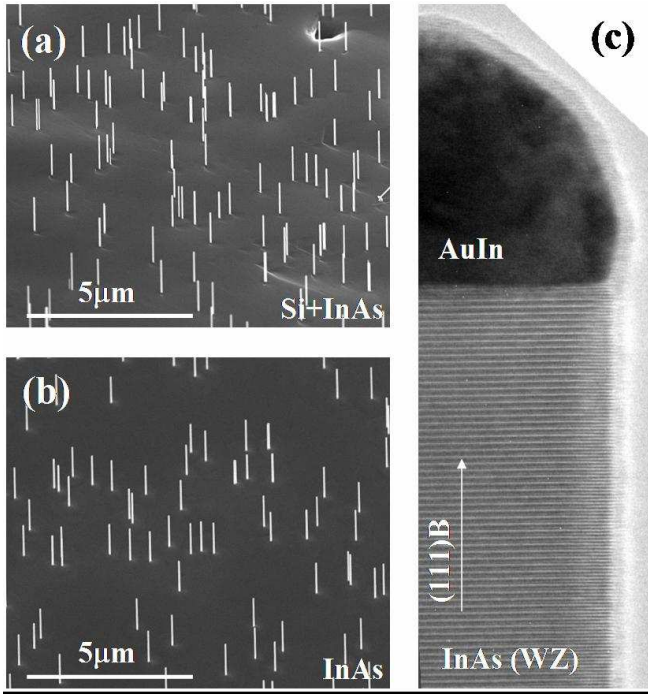


FIG. 5: (a) SEM image of InAs NWs grown on a thick InAs film deposited on Si(111). (b) SEM image of InAs NWs grown on a standard InAs(111)B substrate. Both images were taken at a tilt angle of  $30^\circ$ . (c) High-resolution TEM image of an InAs NW grown on a InAs/Si substrate.

$1.7 \pm 0.15 \mu\text{m}$  and a diameter of  $\approx 65 \text{ nm}$ . This can be compared with the length of  $1.7 \pm 0.1 \mu\text{m}$  obtained on a control InAs(111)B substrate (see Fig. 5b). The negligible statistical difference between the two cases indicates that these engineered substrates can be successfully employed for NW growth. We note that growth of InAs NWs on these layers provides an original tool to detect APDs. Indeed, NWs can only grow vertically with such a high yield on the (111)B surface while one would expect non-vertical growth directions and different growth rates on a (111)A surface [19]. The comparable growth rate and the perfect vertical orientation for InAs/Si(111) and InAs/InAs(111)B samples on large areas demonstrate the almost perfect (111)B orientation of the substrate (Fig. 5a,b). Growth starting from lithographically-defined Au nanoparticles was also investigated and gave good yield of NW arrays (see supplementary material and reference [9] for applications to wrap-gate transistors). In order to gain insight about the quality of the crystal structure of NWs grown on the InAs/Si substrates, high resolution TEM evaluation was performed and compared to the state-of-the-art homoepitaxial InAs NWs grown by CBE. Figure 5c demonstrates that NWs crystallize in the usual hexagonal wurtzite phase, with nearly no stacking faults (density  $\ll 1 \mu\text{m}^{-2}$ ). It can be concluded that the engineered substrate does not affect in any significant

way the nucleation nor the crystal quality of the NWs.

It is worth noting that different approaches for the integration of III-V NWs on Si have been developed in recent times: one example is the direct growth of InAs NWs on Si, a nice demonstration of the flexibility offered by the NW growth technique [20, 21]. The alternative strategy analyzed in this work presents more lattice matching issues but also significant advantages: it eliminates problems related to undesired InAs/Si heterojunctions at the base of the NW, i.e. directly in the conduction path; it provides a natural connection layer that can be patterned to address single devices in a multi-NW chip. In addition to this, other groups demonstrated the growth from *peeled* thin InAs(111)B layers [22]: while such a strategy clearly yields high-quality InAs cap layers, it relies critically on the perfect flatness of the substrate and cannot be used with patterned substrates.

#### IV. CONCLUSIONS

We have demonstrated the controlled growth of InAs NWs starting from two different engineered substrates: a 50 nm-thick InAs cap layer grown on top of a GaAs/AlGaAs heterostructure and a  $2 \mu\text{m}$ -thick InAs buffer layer deposited on a Si(111) wafer. Both substrates offer specific advantages with respect to bulk InAs(111)B. In both cases the top layers can be patterned and allow the selective addressing of single NWs as well as the reduction of stray capacitances to the electrodes in wrap-gate transistor design. Finally, we demonstrated the growth of NWs starting from a GaAs/AlGaAs high-mobility structure designed for the realization of micro-mechanical structures by selective etching.

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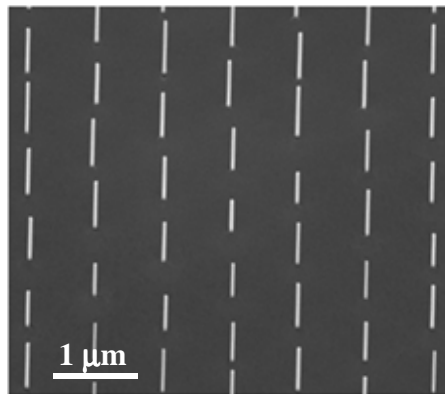
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## Controlled growth of InAs nanowires on engineered substrates. Supplementary material

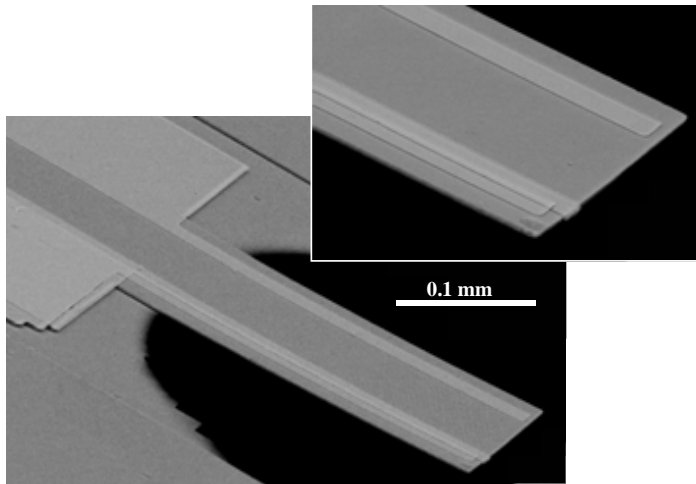
The optimization of NWs growth procedures on engineered substrates opens the way to complex NW-based devices in which the crucial issue of independent and flexible connections to single NWs has to be addressed. In addition, layered substrates make other micro- and nano-structures such as free standing cantilevers possible. In order to demonstrate the viability of these perspectives, we illustrate and present proof of concepts for two of the key steps in the achievement of these long term goals.

**Control of the position of vertical NWs on engineered substrates.** Figure S1 shows an example of NWs arrays grown starting from lithographically-defined Au nanoparticles. In this case we demonstrate the successful growth of an hexagonal array of InAs NWs starting from the (111)B InAs/Si substrate described in the paper. Differently from what happens with normal bulk substrates, engineered samples can be patterned to define NW interconnects. NWs arrays have also been used recently to demonstrate wrap-gated transistor structures (C.Thelander *et al.* IEEE Elect. Dev. Lett. **29**, 206 (2008)).



**Figure S1** – Controlled growth of nanowires on the (111)B InAs/Si substrate described in Section two. Wires form an ordered array grown using Au nanoparticles defined by electron beam lithography. Scanning electron picture taken at 30° degrees tilt angle.

**Free-standing microstructures obtained by selective etching of GaAs/AlGaAs heterostructures.** Figure S2 shows two scanning electron pictures of an example of a cantilever developed at NEST by selective etching of a GaAs/AlGaAs heterostructure similar to the one studied in the paper. Patterned electrodes are visible in the picture and can be readily realized on the cantilever by standard nano as well as microfabrication techniques. Similarly, patterned Au nanoparticles can be defined and used to grow NWs at controlled positions prior to the cantilever definition. Techniques for obtaining cantilever structures are based on standard microfabrication processes, which are compatible with substrates already containing standing NWs, as demonstrated by the successful development of vertical transistors based on arrays of NWs. We thank P.Pingue and V.Piazza for the pictures of the cantilever structure.



**Figure S2** – Demonstration of a 100 micron wide cantilever fabricated by selective etching of an AlGaAs heterostructure with a layer sequence similar to the one used in Section one of the paper.